central processing unit and a direct memory access unit, the interface unit comprising:

a receive channel for receiving data groups from the communication bus and the applying the data groups to the ~~data processing unit~~ direct memory access unit; and

a transmit channel for receiving data groups from the ~~data processing unit~~ direct memory access unit and applying the signal groups to ~~a~~ the communication bus, wherein the interface unit can function in an ATM interface mode and can function in an I/O interface mode.

Please amend Claim 2 as follows.

2. (Currently Amended) The interface unit as recited in claim 1 wherein the interface unit ~~can function is a UTOPIA ATM interface mode and can function in an I/O interface mode~~ the direct memory access unit and the central processing unit are fabricated on the same chip.

Please amend Claim 3 as follows.

3. (Currently Amended) The interface unit as recited in claim ~~1~~ 2 wherein ~~the interface unit exchanges data groups with the direct memory access unit of a~~ the data processing unit includes a plurality of central processing units coupled to the direct memory access unit.

4. (Original) The interface unit as recited in claim 1 further comprising a control register, the control register determining when the interface unit is in the ATM

mode of operations and when the interface unit is in the I/O mode of operation.

5. (Original) The interface unit as recited in claim 1wherein the interface unit includes:

an input interface unit;

an output interface unit;

an input buffer memory unit, wherein the transfer between the input buffer memory unit and the direct memory access unit is determined by a receive event signal; and

an output buffer memory unit, wherein the transfer between the direct memory access unit and the output buffer memory unit is determined by a transmit event signal.

6. (Original) The interface unit as recited in claim 1 wherein the UTOPIA ATM URDATA signal corresponds to an I/O OUTDATAVALID signal, and wherein a UTOPIA ATM UXCLAV signal corresponds to an I/O INDATAVALID signal.

Please amend claim 7 as follows.

7. (Currently Amended) A method of exchanging data groups between a communication bus and a data processing system, the data processing unit including a central processing unit and a direct memory access unit, the method comprising:

in response to a first set of signals in an interface unit, exchanging data groups with the communication bus in a ATM mode of operation; and

in response to a second set of signals in the interface unit, exchanging data groups with the communication bus in an I/O mode of operation.

Please amend Claim 8 as follows.

8. (Currently Amended) The method as recited in claim 7 ~~wherein exchanging data groups includes exchanging data groups in a UTOPIA AMT mode of operation~~ further comprising fabricating the interface unit, the direct memory access unit and the central processing unit on a single chip.

9. (Original) The method as recited in claim 8 wherein the processor is a digital signal processor.

10. (Original) The method as recited in claim 8 further comprising implementing the interface unit including:

an input interface unit;

an output interface unit;

an input buffer memory unit, wherein the transfer between the input buffer memory unit and the direct memory access unit is determined by a receive event signal; and

an output buffer memory unit, wherein the transfer between the direct memory access unit and the output buffer memory unit is determined by a transmit event signal.

Please amend Claim 11 as follows.

11. (Currently amended) The method as recited in claim 10 further including storing the first and the second set of signals in a control register in the interface unit, the stored signals determining when the interface unit is in the ATM mode or is in the I/O mode.

Please amend Claim 12 as follows.

12. (Currently Amended) The method as recited in claim 11 ~~wherein 1~~ wherein the UTOPIA ATM URDATA signal corresponds to an I/O OUTDATAVALID signal, and wherein a UTOPIA ATM UXCLAV signal corresponds to an I/O INDATAVALID signal.

Please amend Claim 13 as follows.

13. (Currently Amended) A data processing unit comprising:

a connector for coupling to a communication bus;

a processor;

a direct memory access unit; and

an interface unit implementing the exchange of data groups between the connector and the ~~processor~~ direct memory access unit; the interface unit including a control register, the interface unit operating in an ATM mode when a first set of signals are stored in the control register, the interface unit operating in an I/O mode when a second set of signals are stored in the control register.

Please amend Claim 14 as follows.

14. (Currently Amended) The data processing system as recited in claim 13 wherein the interface unit, ~~operates in a UTOPIA ATM mode when the first set of signals are stored in the control register~~ the direct memory access unit and the processor are fabricated on a single chip.

15. (Original) The interface unit as recited in claim 13, the interface unit including:

an input interface unit;

an output interface unit;

an input buffer memory unit; wherein the transfer between the input buffer memory unit and the direct memory access unit is determined by a receive event signal; and

an output buffer memory unit, wherein the transfer between the direct memory access unit and the output buffer memory unit is determined by a transmit event signal.

Please amend Claim 16 as follows.

16. (Currently Amended) The data processing unit as recited in claim ~~13~~ 14 wherein the ~~processor~~ data processing unit includes a ~~direct memory access unit, the interface unit coupled between the direct memory access unit and the connector~~ plurality of processors.